

Customer No.: 31561
Docket No.: 13039-US-PA
Application No.: 10/710,672

AMENDMENTS

To the Claims :

1. (original) A method of fabricating a non-volatile memory, comprising the steps of:

providing a substrate;

forming a first dielectric layer over the substrate;

forming a patterned mask layer over the first dielectric layer, wherein the patterned mask layer has a trench;

forming a pair of charge storage spacers on the sidewalls of the trench;

removing the patterned mask layer;

forming a second dielectric layer over the substrate to cover the charge storage spacers and the first dielectric layer;

forming a conductive layer over the second dielectric layer;

patterning the conductive layer to form a gate structure over the charge storage spacers;

removing portions of the second dielectric layer and the underlying first dielectric layer which are not covered by the gate structure; and

forming source/drain regions in the substrate on each side of the gate structure.

2. (original) The method of claim 1, wherein the step of forming the charge

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storage spacers on the sidewalls of the trench comprises:

forming a charge storage material layer over the substrate; and

etching back the charge storage material layer.

3. (original) The method of claim 2, wherein the charge storage material layer is a silicon nitride layer or a silicon oxynitride layer.

4. (original) The method of claim 2, wherein the charge storage material layer comprises a doped polysilicon layer.

5. (original) The method of claim 1, wherein the first dielectric layer comprises a silicon oxide layer.

6. (original) The method of claim 1, wherein the second dielectric layer is an oxide-nitride-oxide composite layer, an oxide-nitride composite layer or a silicon oxide layer.

7. (original) The method of claim 1, wherein after patterning the conductive layer to form the gate structure, further comprises forming a dielectric spacer on the sidewalls of the gate structure.

8. (original) The method of claim 1, wherein the patterned mask layer is a silicon oxynitride layer or a silicon nitride layer.

9. (original) The method of claim 1, wherein the step of removing the patterned mask layer comprises performing an wet etching operation using hot phosphoric acid solution.

10. (original) The method of claim 1, wherein the conductive layer comprises a

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doped polysilicon layer.

11. (original) A method of fabricating a flash memory, comprising the steps of:
providing a substrate;
forming a tunneling dielectric layer over the substrate;
forming a patterned mask layer over the tunneling dielectric layer, wherein the patterned mask layer has a trench;
forming a conductive layer over the substrate to cover the surface of the trench;
removing a portion of the conductive layer to form a pair of conductive spacers on the respective sidewalls of the trench to serve as floating gates;
removing the patterned mask layer;
forming an inter-gate dielectric layer over the substrate to cover the floating gates and the tunneling dielectric layer;
forming a control gate over the inter-gate dielectric layer above the conductive spacers; and
forming source/drain regions in the substrate on each side of the control gate.
12. (original) The method of claim 11, wherein the tunneling dielectric layer comprises a silicon oxide layer.
13. (original) The method of claim 11, wherein the patterned mask layer is a silicon oxynitride layer or a silicon nitride layer.
14. (original) The method of claim 11, wherein the inter-gate dielectric layer is an oxide-nitride-oxide composite layer, an oxide-nitride layer or a silicon oxide layer.

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15. (original) The method of claim 11, wherein the conductive layer comprises a doped polysilicon layer.

16. (original) The method of claim 13, wherein the step of removing the patterned mask layer comprises performing a wet etching operation using hot phosphoric acid solution.

17. (original) The method of claim 10, wherein after forming the control gate over the inter-gate dielectric layer, further comprises:

forming a pair of dielectric spacers on the sidewalls of the control gate; and

removing portions of the inter-gate dielectric layer and the tunneling dielectric layer by using the dielectric spacers and the control gate as hard masks.

18. (withdrawn) A method of fabricating a silicon-oxide-nitride-oxide-silicon (SONOS) memory, comprising the steps of:

providing a substrate;

forming a bottom silicon oxide layer over the substrate;

forming a patterned mask layer over the bottom silicon oxide layer, wherein the patterned mask layer has a trench;

forming a charge-trapping layer over the substrate to cover the surface of the trench;

removing a portion of the charge-trapping layer to form a pair of charge storage spacers on the sidewalls of the trench;

removing the patterned mask layer;

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forming a top silicon oxide layer over the substrate to cover the pair of charge storage spacers and the bottom silicon oxide layer;

forming a gate over the top silicon oxide layer above the pair of charge storage spacers; and

forming source/drain regions in the substrate on each side of the gate.

19. (withdrawn) The method of claim 18, wherein the patterned mask layer is a silicon oxynitride layer or a silicon nitride layer.

20. (withdrawn) The method of claim 18, wherein the charge-trapping layer is a silicon nitride layer or a silicon oxynitride layer.

21. (withdrawn) The method of claim 18, wherein after forming the gate over the top silicon oxide layer, further comprises:

forming a pair of dielectric spacers on the sidewalls of the gate but exposing the top silicon oxide layer; and

removing portions of the top silicon oxide layer and the underlying tunneling dielectric layer by using the dielectric spacers and the gate as hard masks;